SEP-400A

Spectral Energy Processor

CRL CIRCUIT RESEARCH LABS, INC.

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WARRANTY

Circuit Research Labs, Incorporated warrants its products to be free of defects in materials and/or workmanship. This warranty shall extend for a period of one (1) year from the date the product was originally shipped.

Circuit Research Labs' warranty does not apply to products that have been damaged due to and/or subjected to improper handling by shipping companies, negligence, accidents, improper use, or alterations not authorized by Circuit Research Labs, Incorporated.

THIS WARRANTY IS IN LIEU OF AND EXCLUDES ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED AND IN NO EVENT SHALL CIRCUIT RESEARCH LABS, INCORPORATED BE LIABLE FOR ANY ANTICIPATED PROFITS, INCIDENTAL OR CONSEQUENTIAL DAMAGES, LOSS OF TIME OR OTHER LOSSES INCURRED BY THE BUYER/CUSTOMER IN CONNECTION WITH THE PURCHASE, OPERATION OR USE OF THE PRODUCT.

CHAPTER I

SEP-400A

SPECTRAL ENERGY PROCESSOR

1.0 INTRODUCTION

Circuit Research Labs has created a precision multiband gain controller that will give you precise dynamic control and equalization of the sound of your program material - the SEP-400A, Spectral Energy Processor.

The heart of the SEP-400A is the Dynamic Energy Processor (DEP) section. This processor controls the overall loudness of your program material by front panel adjustments.

The program material first enters a unique four channel equalizer splitting network which divides the program material into four logarithmically equal bands. These four bands have been especially selected to bring out the advantages of each of the frequency ranges. Each band contains a sophisticated gain control element with a program control module which will regulate the program dependent action of the AGC attack and release time circuits. Custom tailoring of the output frequency response of the four bands is easily achieved by adjusting the front panel controls L, M1, M2 and H. These are actually output level controls of the four AGC bands.

An important feature of the SEP-400A is its ability to increase program loudness without creating unwanted non-musical distortions as found with other processors on the market.

A programmable gate threshold has been included to aid in keeping unwanted background noise levels low during program pauses. This gate can be set high, low or off by one rear panel control.

Circuit Research Labs has increased the versatility of the SEP-400A by including the Peak Energy Processor. The Peak Energy Processor (PEP) is a special application device. This unconventional peak limiter will alter the gain of the program peaks while monitoring the average loudness. This special purpose processor is an added aid for deficient or older AM transmitters.

The SEP-400A is, through its sophisticated circuitry and unique design, the most versatile of processcrs. It will add consistency of sound and loudness control which competitive broadcast stations require.

1.1 PREVENTIVE MAINTENANCE

A minimum amount of preventive maintenance is required to insure optimum performance of the SEP-400A processor. If you do not have a regular preventive maintenance schedule in existance Circuit Research Labs suggests the following check list be performed once a week.

1. Check to insure that the input and output cables are secured tightly to their respective terminals and are not frayed.
2. Check to insure that all knobs, switches and indicators are secure.
3. Check to insure that there is not a build up of dirt or dust on or around the SEP-400A.

NOTE

It is recommended that no liquids such as coffee, water etc. be placed on the SEP-400A. Accidental spillage could result in serious damage to the unit.

1.2 RETURN FOR REPAIR POLICY

In the event that the SEP-400A must be returned to the factory for in warranty and/or out of warranty repair, Circuit Research Labs requires that a Return Authorization (RA) Number be attached to the unit. In order to insure prompt service and quick turn around time for equipment repair, Circuit Research Labs requires that the following information be included when the unit is returned to the factory:

1. Return Authorization Number affixed to the outside of shipping container.

NOTE

The RA Number is obtained by calling or writing Circuit Research Labs, Incorporated.

2. Description of trouble - This will help the Repair Department in diagnosing the trouble faster. This description should include what mode of operation the unit was in when the trouble was detected and the system configuration being used.
3. Serial Number of the unit and approximate date of purchase - This will aid in the determination of billing for warranty or out of warranty repair.

Circuit Research Labs requests that all units being shipped back to the factory be shipped via United Parcel Service (UPS) to: Circuit Research Labs Inc., 3204 South Fair Lane, Tempe, Arizona 85282.

CHAPTER II

INSTALLATION

2.0 INITIAL SET UP

2.1 INITIAL SWITCH POSITIONS

2.1.1 General

Before operating the SEP-400A Spectral Energy Processor, the front and rear panel controls must be set so the starter/calibration procedure can be completed.

2.1.2 Front Panel Controls (Figure 2-1)

Table 2.1 shall define the position of the front panel controls of the SEP-400A.

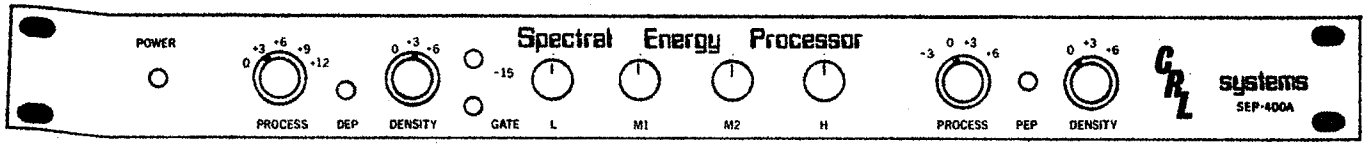


FIGURE 2-1 FRONT PANEL CONTROL LOCATIONS

TABLE 2.1 FRONT PANEL CONTROL POSITIONS

Control	Position
Process (DEP)	Set to the +6 position
Density (DEP)	Set to the +3 position
L	Set to the vertical position
M1	Set to the vertical position
M2	Set to the vertical position
H	Set to the vertical position
Process (PEP)	Set to the 0 position
Density (PEP)	Set to the +3 position

2.1.3 Rear Panel Controls (Figure 2-2)

Table 2.2 shall define the position of the rear panel controls of the SEP-400A.

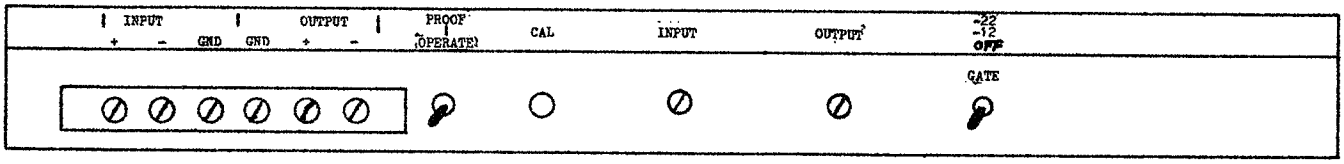


FIGURE 2-2 REAR PANEL CONTROL LOCATIONS

TABLE 2.2 REAR PANEL CONTROL POSITIONS

Control	Position
PROOF/Operate Switch	Set to the Operate position
Input Calibration Control	Factory pre-aligned for direct connection to the other CRL input and output units
Output Control	
Gate Switch	Set to the -22db position

2.2 INTERCONNECTIONS

2.2.1 General

The SEP-400A may be wired for either balanced or unbalanced operation. Paragraphs 2.2.2 and 2.2.3 shall define the connections procedure required for the balanced or unbalanced mode of operation respectively. Determine if your system is balanced or unbalanced and proceed with the applicable set of instructions.

2.2.2 Balanced Operation (Figure 2-3)

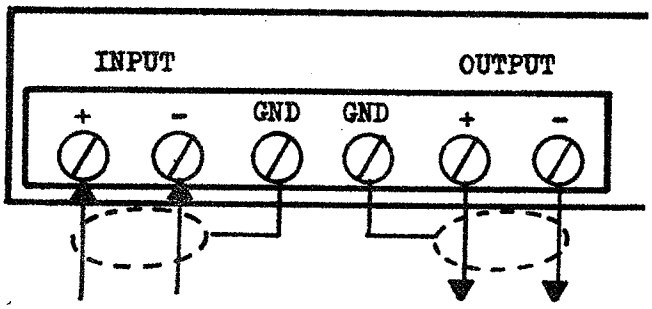


FIGURE 2-3 BALANCED OPERATION DIAGRAM

The following procedure shall define the interconnections that are required for the SEP-400A to operate in the balanced mode of operation.

NOTE

All interconnect cables should be shielded for best operation.

1. Connect the balanced audio OUTPUT cable from the CRL preparation processor or other audio source to the terminals labeled INPUT on the SEP-400A.
2. Connect the balanced audio INPUT cable from the CRL AM Peak Modulation Controller or FM Stereo Modulation Processor or recording equipment to the terminal labeled OUTPUT on the SEP-400A.
3. Connect the shield of the cable connected to the SEP-400A INPUT to the Ground (GND) terminal closest to the INPUT terminals.
4. Connect the shield of the cable connected to the SEP-400A OUTPUT terminal to the Ground (GND) terminal closest to the OUTPUT terminal.

NOTE

It is imperative that both ends of the interconnect cables' shield be connected to Ground.

2.2.3 Unbalanced Operation (Figure 2-4)

The following procedure shall define the interconnections that are required for the SEP-400A to operate in the unbalanced mode of operation.

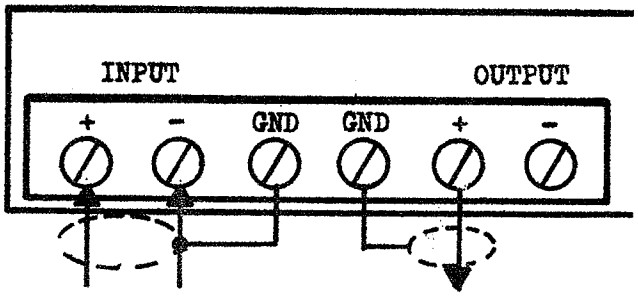


FIGURE 2-4 UNBALANCED OPERATION DIAGRAM

NOTE

All interconnect cables should be shielded for best operation.

1. Connect the unbalanced audio OUTPUT cable from the CRL preparation processor or other audio source to the plus (+) INPUT terminal on the SEP-400A.
2. Using a short section of wire, connect the minus (-) INPUT terminal of the SEP-400A to the Ground (GND) terminal closest to the INPUT terminal.
3. Connect the shield of the cable connected to the SEP-400A INPUT to the Ground (GND) terminal closest to the INPUT terminals.
4. Connect the shield of the cable connected to the SEP-400A OUTPUT to the Ground (GND) terminal closest to the OUTPUT terminals.
5. Connect the signal lead of the cable to the SEP-400A plus (+) OUTPUT terminal.

NOTE

For unbalanced operation the minus (-) OUTPUT terminal must not be grounded. This output is directly coupled to the output of an amplifier and is not transformer coupled.

2.3 CALIBRATION

2.3.1 General

Once the front and rear panel controls are set and the rear panel interconnections are made, the SEP-400A input calibration may be checked.

Paragraph 2.3.2 shall define the calibration procedure when using a CRL system. Paragraph 2.3.3 shall define the calibration procedure when using the SEP-400A in a system comprizing auxilary equipment.

2.3.2 CRL System Calibration

1. Place the pink noise generator on the APP-400 or SPP-800 in the "ON" position.
2. Rotate the input control located on the rear panel, clockwise, until the calibration Light Emitting Diode (LED) just begins to light.

2.3.3 Auxilary Equipment Calibration

1. Set the auxilary equipment for 0dbm output.
2. Rotate the input control located on the rear panel of the SEP-400A, clockwise, until the "Cal" Light Emitting Diode (LED) just begin to flash on program peaks approximately 10-20% of the time.

2.4 CALIBRATION DEVIATIONS

2.4.1 General

The SEP-400A is shipped from the factory with the input attenuators set at an input gain range of +5dbm to -15dbm for AM and +15dbm to 0dbm for FM. If during calibration, the input control is turned over 75% of its range, reduce the sensitivity setting of the input attenuators to the -10 to -30dbm settings. If during the calibration procedure the input control is turned under 25% of its range the sensitivity setting must be increased to the +15 to 0dbm setting. Table 2.3 will define the proper switch settings for adjusting the gain range of the SEP-400A to the medium or high sensitivity setting.

NOTE

In the following table and procedures the term "ON" will mean the switch is in the closed position and the term "OFF" will mean the switch is in the open position.

TABLE 2.3 ATTENUATOR SWITCH POSITIONS

Gain Range	Switch Setting			
	S1	S2	S3	S4
High Sensitivity Setting (-10 to -30dbm)	On	On	On	On
Medium Setting (+5 to -15dbm)	Off	Off	On	On
Minimum Sensitivity Setting (+15 to 0dbm)	Off	Off	Off	Off

2.4.2 If the calibration LED does not begin to flash until after the calibration control has been rotated over 75% of its range or under 25% of its range, proceed as follows:

1. Remove power from the SEP-400A.
2. Rotate the calibration control completely counterclockwise.
3. Remove the top cover of the SEP-400A.
4. Locate the internal mini dip switches. (Refer to Figure 2-5 for switch location)
5. Place switches S1, S2, S3 and S4 in the pattern defined in Table 2.3 for the sensitivity setting required.
6. Replace the top cover of the SEP-400A.
7. Apply power to the SEP-400A.
8. Check the audio console or other programming source to insure the proper reference output has not drifted if using the Auxilary Equipment Calibration, or that the pink noise generator is "ON" if using the CRL System Calibration.
9. Turn the input control until the LED just comes on if using the CRL System Calibration or flashes on program peaks 10-20% of the time if using the Auxilary Equipment Calibration.

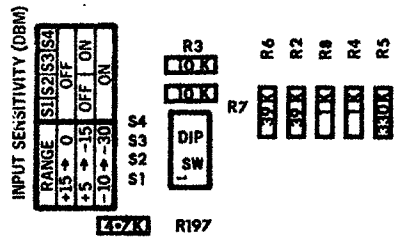


FIGURE 2-5 ATTENUATOR SWITCH LOCATIONS

CHAPTER III

OPERATION

3.0 GENERAL OPERATIONAL THEORY

The SEP-400A contains two processors in one unit. The first processor contains the input amplifier, four band Dynamic Energy Processor and equalization network and the summer amplifier. The second processor contains the Peak Energy Processor and the output amplifier.

When the program material enters the Dynamic Energy Processing circuitry, it first enters a four channel equalizer network where overall program loudness can be controlled by the front panel controls. The program material is divided into four electro-acoustically chosen bands. The four bands were chosen for their logarithmically equal spacing through the audible frequency range and to separate the musical instrument bands of bass and high frequencies apart from the human voice band. In addition to these divisions, the human voice band was further divided into the vowel or fundamental harmonics band and the consonant or presence and intelligibility band. The attack and release times of all four channels are controlled by analog computer circuits. These circuits produce the complex program dependent attack and release times from the measurement of program density, frequency content, transient content, and average to peak level ratio. While the processing is automatically program controlled, the range of the automatic control can be varied. The ability to control this range is the function of the DEP density switch on the front panel.

The four front panel controls marked L, M1, M2, and H are the output controls of the four DEP bands and are made to be used as a four band equalizer for setting the "output" sound of the unit.

The audio signal is then recombined in the summer amplifier where it is transferred to the Peak Energy Processor circuitry. The Peak Energy Processor circuitry will perform the final adjustments of the program material before it is transmitted. The amount of peak to average energy content will be set in this stage.

When operating the SEP-400A special attention must be taken in the

adjustment of the controls. All major adjustments should be made in the DEP section of the processor.

The equalization controls should not exceed the high and low limits that are indicated on the front panel. If it is required to exceed these limits readjust the DEP section.

The PEP section of the SEP-400A should be used for minor signal adjustment. It is recommended that the PEP process control be set at zero (0) and the PEP density control be set at the +3 or the +6 position for on the air operation for most applications.

3.1 FRONT PANEL CONTROLS

3.1.1 Dynamic Equalization Process (DEP) Process Control Switch (Figure 3-1)

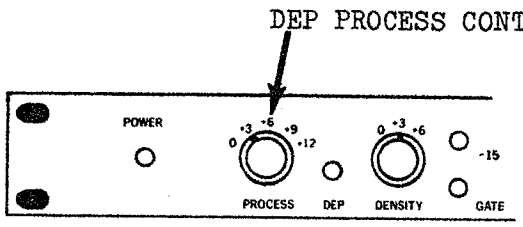


FIGURE 3-1 DEP PROCESS CONTROL SWITCH LOCATION

The amount of processing in the DEP section is controlled by the front panel DEP process switch. After input level calibration has been initially performed, the desired level of four channel processing can be adjusted in 3db steps from 0 to 12db. The process switch is a precision step type which controls the total input level to all bands and therefore allows for repeatable levels of processing.

By rotating the switch clockwise you will notice an increase in loudness. The loudness increase will be the greatest when the switch is changed from the 0 to +3 position and from the +3 to +6 position. As the switch is turned further clockwise the loudness increase is less than the preceeding step.

Use minimum process level and maximum density for maximum loudness increase with still apparent dynamic integrity. Maximum process and minimum density should be used for maximum dynamic equalization effect.

NOTE

This control is very effective in re-equalizing spectrally deficient program material.

3.1.2 Dynamic Equalization Processor (DEP) Density Control Switch (Figure 3-2)

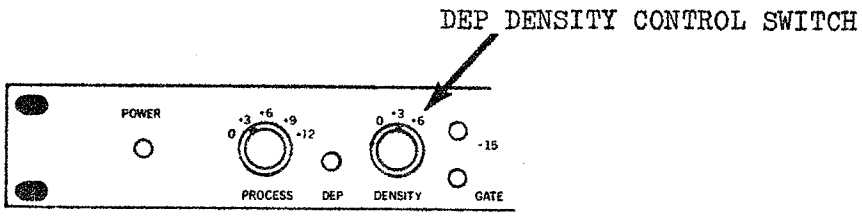


FIGURE 3-2 DEP DENSITY CONTROL SWITCH LOCATION

The DEP density control switch controls the attack and release times acting upon the audio transients within the incomming signal. By increasing the attack and release times, which are generated by analog computers, the RMS energy of the audio signal is increased. The attack and release times are derived from the system measurement of program density, frequency content, and the average to peak level ratio of the audio signal. By analyzing all three functions, in the analog computer, during actual signal processing the RMS energy will remain constant. The three density positions, 0, +3 and +6 produce three different actions on the audio signal. With the switch in the zero (0) position the four bands operate primarily as dynamic equalizers which maintain consistant sound equalization. When the switch is in the +3 position the four bands resemble AGC/compression type devices and operate on reducing long term and medium dynamic ranges. In the +6 position the four bands become more radical and similiar to compression/

limiting type devices which operate heavily on medium dynamic range reduction.

The DEP density switch is very effective in increasing the RMS energy of your program material without any unpleasant side affects. However, since a loudness increase may result in a loss of dynamic integrity this switch should be set in as low a position as possible to achieve your goal.

3.1.3 Equalization Controls (Figure 3-3)

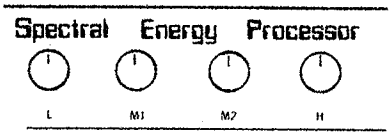


FIGURE 3-3 EQUALIZATION CONTROL LOCATIONS

The four equalization controls will adjust the remix of each of the audio bands in the SEP-400A. These four controls act as a four band equalizer and can be used to adjust the programming so that specific ON-AIR sound can be tailored to your station's requirements. The controls are labeled L for low band, M1 for low-mid range, M2 for high-mid range and H for the high range. These bands, which are logarithmically equal, have gentle 6db per octive cross over points. The cross over points of the four frequency bands are as follows:

The L band will crossover to the M1 band at 100Hz

The M1 band will crossover to the M2 band at 700Hz

The M2 band will crossover to the H band at 5KHz

When adjusting these controls, special attention must be taken to not normally exceed the upper and lower limit markings on the front panel. If your sound requirements demand that the controls exceed the

the limits, reset the controls to the normal position and either reduce or increase the DEP process switch one position.

3.1.4 Peak Energy Processor (PEP) Process Control Switch (Figure 3-4)

PEP PROCESS CONTROL SWITCH

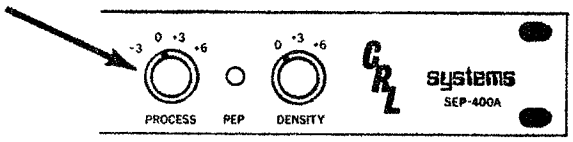


FIGURE 3-4 PEP PROCESS CONTROL SWITCH LOCATION

The PEP process switch is the final and most powerful control of the computer controlled gain processors in the SEP-400A. This switch controls the peak to average energy level of the processed audio. This is done by controlling the gain reduction that can take place in the final wide band gain controller circuits. This switch, in effect, acts like a wide band "peak" limiter. It will limit the amount of signal overshoot without clipping when the pre-determined level is exceeded. When the process switch is set in the +6 position, for example, the gain control circuits are instructed to reduce the peak to average ratio of the summed audio 6db. By rotating the control clockwise, the average to peak output becomes closer to the same value. This will allow the energy content of the signal to increase thus creating an increase in loudness. Since this control is radically effective in reducing the average to peak ratio of the signal, it is recommended that the switch be set to the zero (0) position for most natural sounding audio.

NOTE

A -3 setting of this switch will effectively remove PEP processing.

3.1.5 Peak Energy Processor (PEP) Density Control Switch (Figure 3-5)

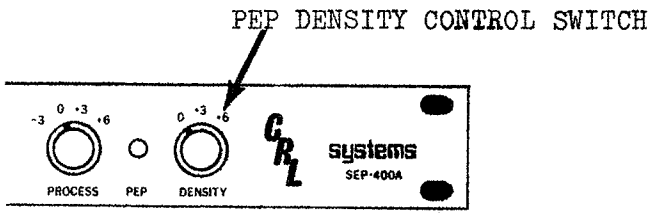


FIGURE 3-5 PEP DENSITY CONTROL SWITCH LOCATION

The PEP density switch controls the PEP PCM module attack and release time ranges. This switch determines how fast the PCM module in the PEP stage will recognize a shift in the average level of the signal. This control, in effect, will maintain a constant ratio of peak energy to average energy of the signal. By placing this switch in a higher numeric value, as shown on the front panel, the ratio of the peak to average energy is decreased. As the ratio is decreased the net effect is to increase the RMS energy present in the audio signal. To obtain optimum performance we suggest that the PEP density switch be placed in the +3 or +6 position and the PEP process switch be placed in the zero (0) position. The density switch, when turned clockwise, will increase the loudness of the audio signal but it is highly recommended that this switch not be used to set your loudness level.

3.2 REAR PANEL CONTROLS

3.2.1 PROOF/Operate Switch (Figure 3-6)

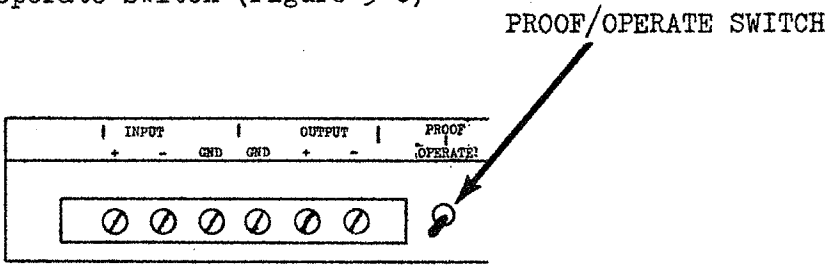


FIGURE 3-6 PROOF/OPERATE SWITCH LOCATION

The PROOF/Operate switch connects the input amplifiers to the output amplifiers. Frequency response and distortion measurements may have to be made in some applications (mainly broadcast). To obtain the correct data the automatic gain control circuits must be defeated. To do this place the PROOF/Operate switch into the PROOF position.

3.2.2 Gate Switch (Figure 3-7)

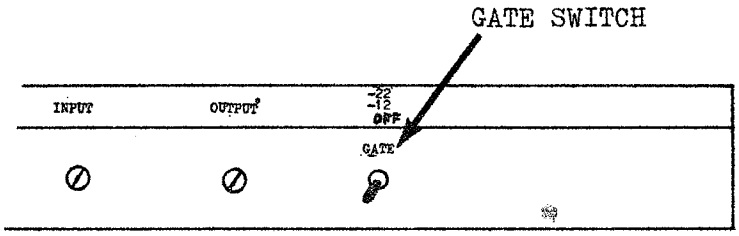


FIGURE 3-7 GATE SWITCH LOCATION

The gate switch will prevent low level signals, such as noise, from being treated as intelligence by the AGC circuits. The gate switch may be set in one of three positions, -22db, -12db or Off. When the input level drops below the threshold determined by the gate switch setting, all

gain control circuits will freeze. For example, if the gate switch is set at -22db, as input signal falls below that threshold, the gain of the output will remain constant until the incoming signal level increases above the threshold again. The gate lamp located on the front panel will illuminate whenever there is a program pause or the input level falls below the preset threshold gate level.

NOTE

CRL suggests the gate switch be set at -22db for most applications.

3.2.3 Output Control (Figure 3-8)

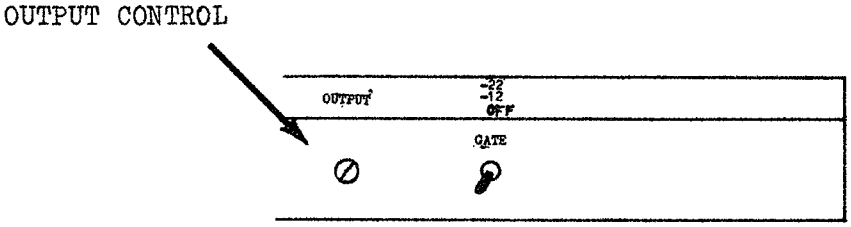


FIGURE 3-8 OUTPUT CONTROL LOCATION

The output control adjusts the recombined output level of the SEP-400A. The control is factory preset for a Odbm output for factory pre-calibrated direct connection to the CRL AM Peak Modulation Controller or the FM Stereo Modulation Processor.

NOTE

Turning the output control completely counterclockwise reduces the output to no signal.

3.2.4 Input Control (Figure 3-9)

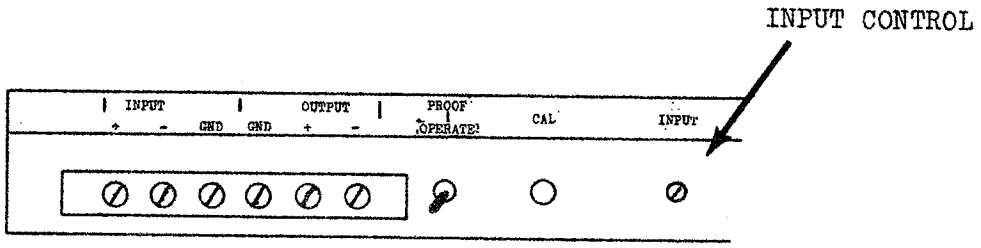


FIGURE 3-9 INPUT CONTROL LOCATION

The input control is used to adjust the amount of input signal that will reach the input amplifier of the SEP-400A and is factory pre-calibrated for direct connection to the output of the CRL Preparation Processors.

3.3 INTERNAL OPTIONS

3.3.1 Input Sensitivity Setting (Figure 3-10)

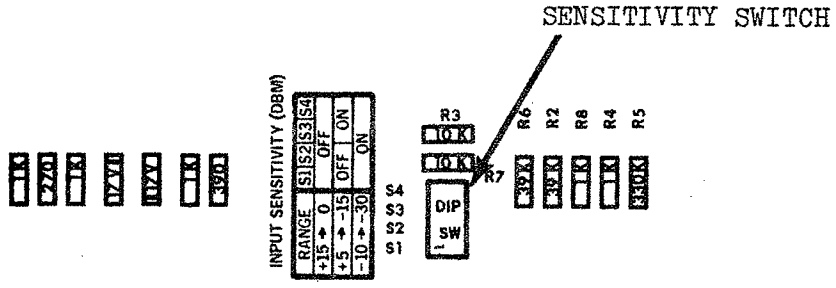


FIGURE 3-10 INPUT SENSITIVITY SETTING

The input sensitivity of the SEP-400A is controlled by a four position mini dip switch. This mini dip switch will select three overlapping gain ranges. These gain ranges are -10dbm to -30dbm, +5dbm to -15dbm and +15dbm to 0dbm. For detailed information concerning the setting of the three gain ranges, refer to Paragraph 2.4, Calibration Deviation Procedure.

3.3.2 Switchable Transient Limiter Circuits (Figure 3-11)

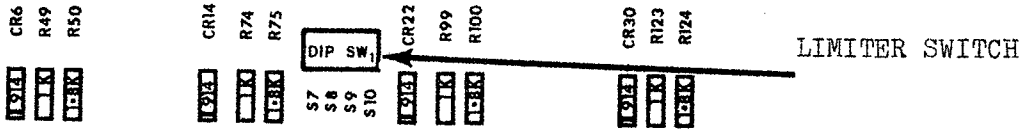


FIGURE 3-11 SWITCHABLE TRANSIENT LIMITER CIRCUITS

The transient limiter circuits located within the SEP-400A, contain a four section mini dip switch. This mini dip switch will cause the band it is associated with to increase the attack time on transients. By increasing the attack time of the transients the program material will be more compressed, thus producing a less dynamic sound. The switches are labeled S7 for the L band, S8 for the M1 band, S9 for the M2 band and S10 for the H band are preset at the factory as shown in Table 3.1.

TABLE 3.1 LIMITER SWITCH POSITIONS

Switch	Position
S7	Off
S8	On
S9	On
S10	Off

If you prefer a more compressed sound on all bands simply place all the switches in the ON position.

3.4 INDICATORS (EXTERNAL) (Figure 3-12)

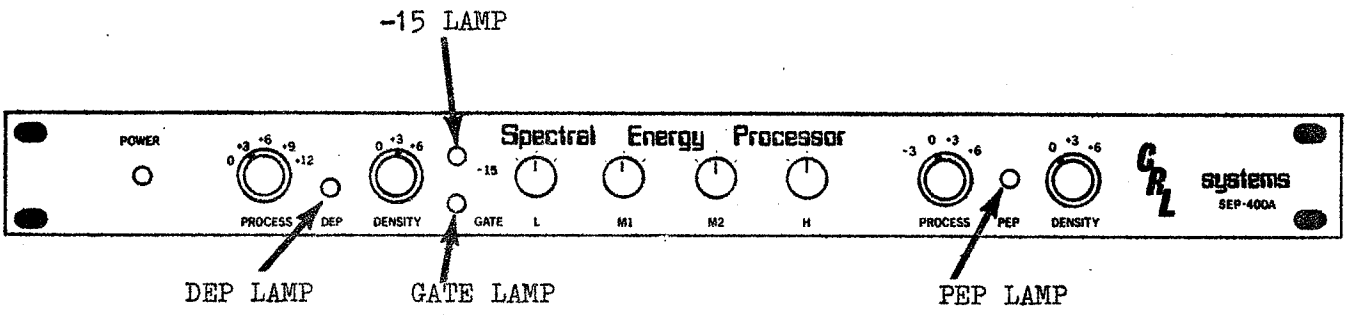


FIGURE 3-12 EXTERNAL INDICATORS

3.4.1 Gate Lamp

The gate lamp will illuminate whenever the SEP-400A freezes the Automatic Gain Control circuits in the four bands and is converted to the linear mode of operation.

3.4.2 -15 Lamp

The -15 lamp will illuminate whenever the program material drops 15db below the preset processing level.

3.4.3 DEP Lamp

The DEP lamp will illuminate whenever there is any gain reduction activity occurring in the DEP section of the SEP-400A.

3.4.4 PEP Lamp

The PEP lamp will illuminate whenever there is any gain reduction activity occurring in the PEP section of the SEP-400A.

3.5 INDICATORS (INTERNAL)

3.5.1 Power Supply Status (Figure 3-13)

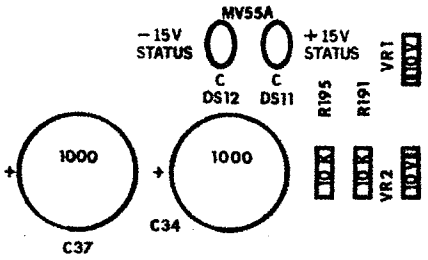


FIGURE 3-13 POWER SUPPLY STATUS

Two LED's, DS-11 and DS-12, monitor the output voltage of the SEP-400A's internal power supply. Should the -15VDC supply fail LED DS-12 will dim or go out, and if the +15VDC supply fails LED DS-11 will dim or go out.

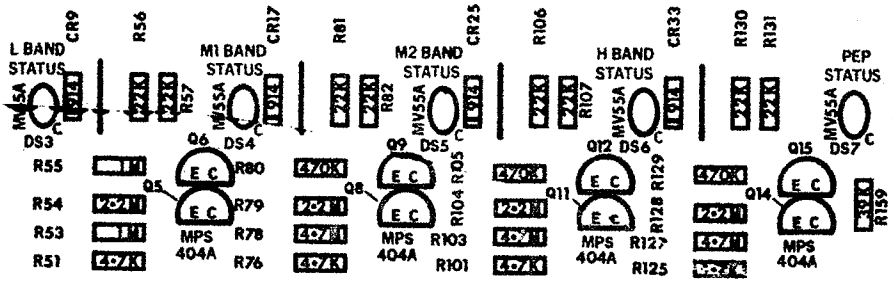


FIGURE 3-14 PEP LAMP AND EQUALIZATION LAMP LOCATIONS

3.5.2 PEP Status (Figure 3-14)

The PEP status lamp is normally lit and will dim whenever there is any gain reduction activity in the PEP section of the SEP-400A.

3.5.3 Equalization Lamps (Figure 3-14)

The four AGC status lamps are normally lit and will dim whenever there is any gain reduction activity occurring in the band the lamp represents.

3.6 PROOF OPERATIONS

3.6.1 Defeating Gain Control

Frequency response and distortion measurements may have to be made in some applications (mainly broadcast). To obtain the correct data the Automatic Gain Control circuits must be defeated. To do this place the operation switch into the PROOF position, and for unity gain set the DEP process switch to full (+12).

WARNING

Return both switches to their previous settings after performing any testing.

CHAPTER IV

THEORY OF OPERATION

4.0 SIMPLIFIED THEORY OF OPERATION (Refer to Block Diagram Figure 4.1)

The external audio signal enters the SEP-400A through the balanced audio input terminals located on the rear panel. The audio input is adjusted by the rear panel INPUT CAL POT, which is used to set the unit's input reference level before entering the INTERNAL INPUT ATTENUATION SWITCHES.

The INTERNAL INPUT ATTENUATION SWITCHES are used to adjust the overall input sensitivity to one of three ranges. These ranges are High (-10 to -30dbm), Medium (+5 to -15dbm) and Low (+5 to 0dbm). Input sensitivity is factory selected at the Medium range.

The input signal then enters the DEP process switch. This switch is set up in 3db steps and is used as an attenuator to drive the signal into the proper amount of gain reduction or compression in the following four independent AGC control amplifiers.

Following the DEP process switch, the audio enters the frequency splitter stage which consists of four passive filters. These filters split the audio into four separate bands which have been selected to give the maximum in quality processing. These band pass ranges are the Bass band labeled "L" on the front panel control, Vocal resonance band labeled M1, Vocal intelligibility or presence band labeled M2 and finally the musical High band labeled H. These four band encompass the audible frequency range of 40 - 15KHz, with the split frequencies of 100Hz separating the L from the M1 band, 700Hz separating the M1 and M2 bands and 5KHz separating the M2 from the H band. These separation points are 3db down in the filtering network.

Dynamic ranges in the four bands are separately reduced or compressed by four independent gain reduction stages. The gain reduction action is controlled by complex gain determining signals derived from the audio bands themselves. Convenient user selection over the operating speeds by the use of the DEP density switch allows even more flexibility for each particular format.

The three position DEP density switch independently tailors

the overall response of the bands. When placed in the 0 (Slow) position the gain reduction stages act as mild AGC's, when placed in the +3 (Medium) position they act as medium speed compressors, and in the +6 (Fast) position they act as high speed compressors. In addition, overshoot limiters may be internally selected for greater control over any or all of the bands which control the audible frequency spectrum. These overshoot limiters cause further compression and tighter control of the audio spectrum in the individual AGC circuits when they are used.

The outputs of the four bands are then fed to the output controls labeled L, M1, M2 and H. These controls equalize the four ranges to the tonal balanced desired by the user.

The summation amplifier next combines the four frequency bands to form the independently band controlled and frequency tailored audio spectrum. After the signal is recombined it then enters the Peak Energy Processing or peak compressor stage. This stage will either allow you to bypass the action of the wide band Peak Energy Processor or allow upto 6db of wide band compression. This is the most radical stage of the SEP-400A. The PEP process switch controlls the amount of drive entering the peak compressor. The PEP process switch has four settings, -3, 0, +3 and +6. However, it is recommended that the PEP process switch be set at 0db. The three position PEP density switch, labeled 0, +3 and +6, sets the slow, medium and fast attack and release times. It is recommended the DEP density switch be set at +3 or +6. The +6 position should be used by those who demand the absolute maximum in audio loudness and are willing to sacrifice dynamic integrity of the audio signal.

The audio signal is now sent to the variable output control, where the level at the output can be continuously selected from off to in excess of 10dbm. This control drives the final balanced output stage which contains a balanced push-pull unity gain amplifier that is required to drive succeeding equipment.

ADDITIONAL FEATURES:

CRL has designed unique indicators for the front and rear panel

of the SEP-400A. These indicators allow the user to monitor gain reduction activity and the Automatic Gain Control circuits.

The Gate LED illuminates whenever the SEP-400A freezes the Automatic Gain Control circuits in the four bands and is converted to the linear mode of operation. The -15 LED illuminates whenever the input audio becomes greater than -15db below the input gain reduction threshold. The DEP LED illuminates whenever there is any gain reduction activity occurring in any of the four bands of the DEP section of the SEP-400A. The PEP LED illuminates whenever the Peak Energy Processor is experiencing any gain reduction activity. The preceding LED's, -15, PEP, DEP and Gate, are all located on the front panel.

The Cal LED, which is the only LED located on the rear panel, illuminates when the signal reaches the gain reduction input threshold reference level of Odb.

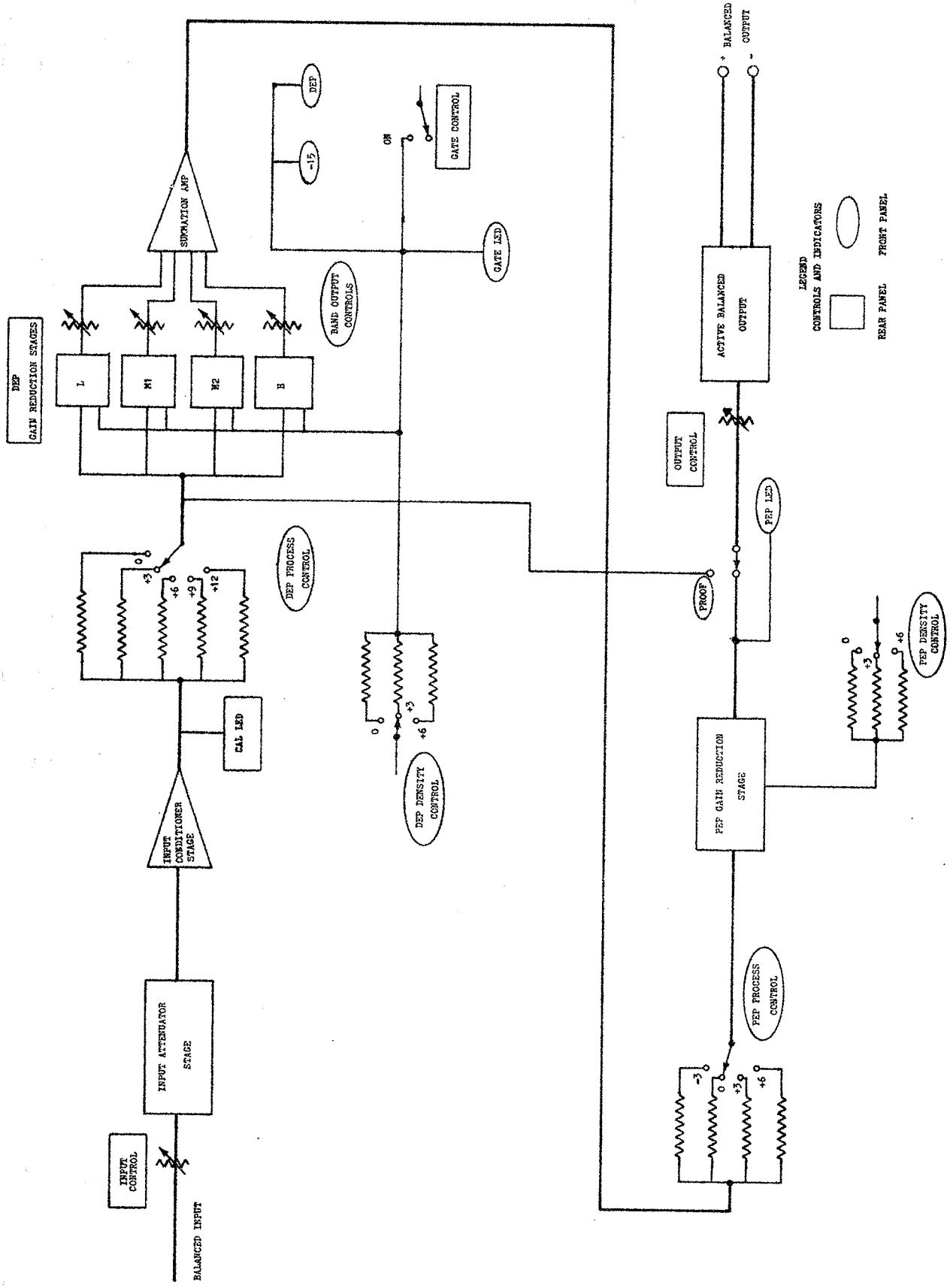
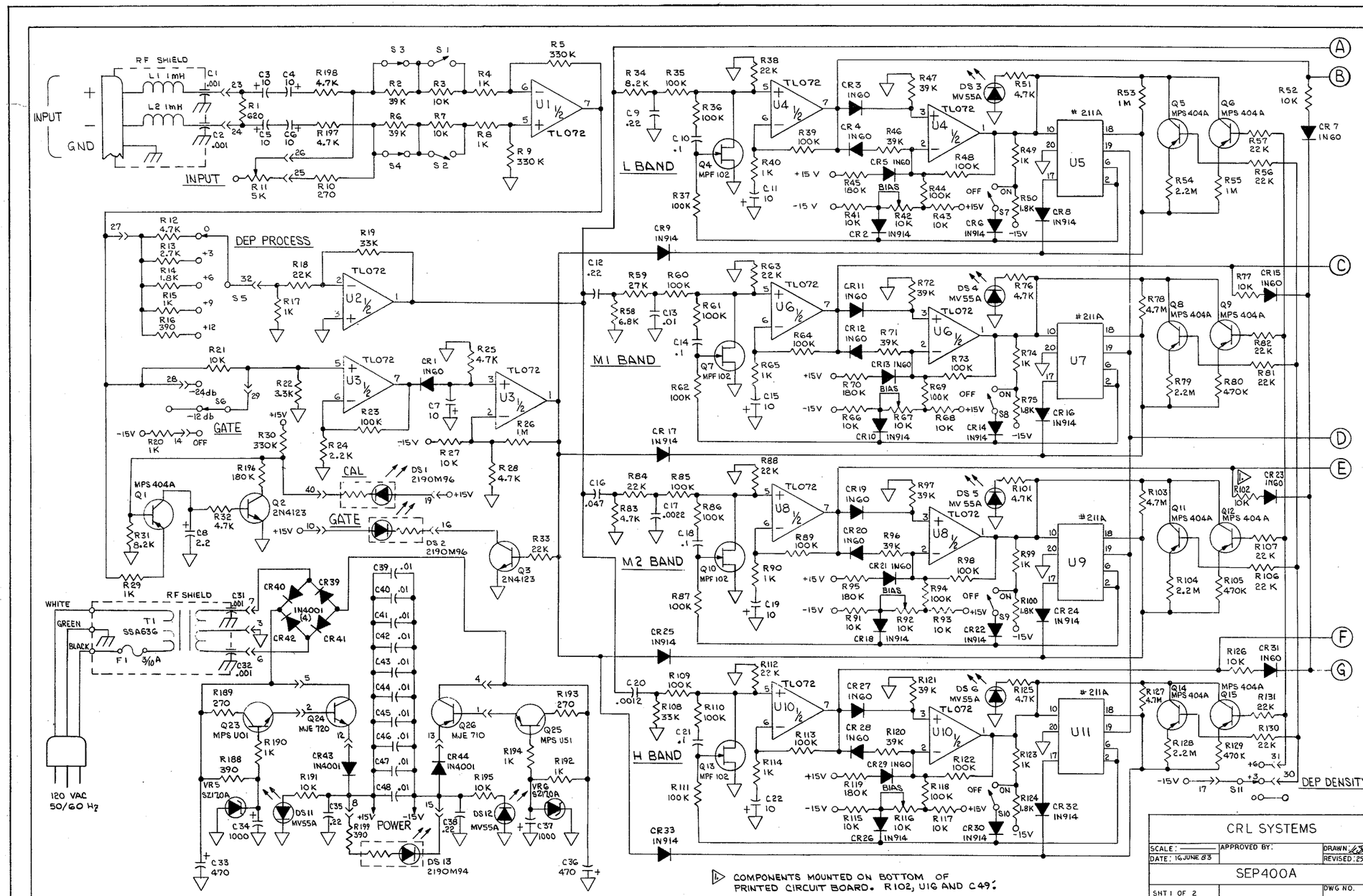
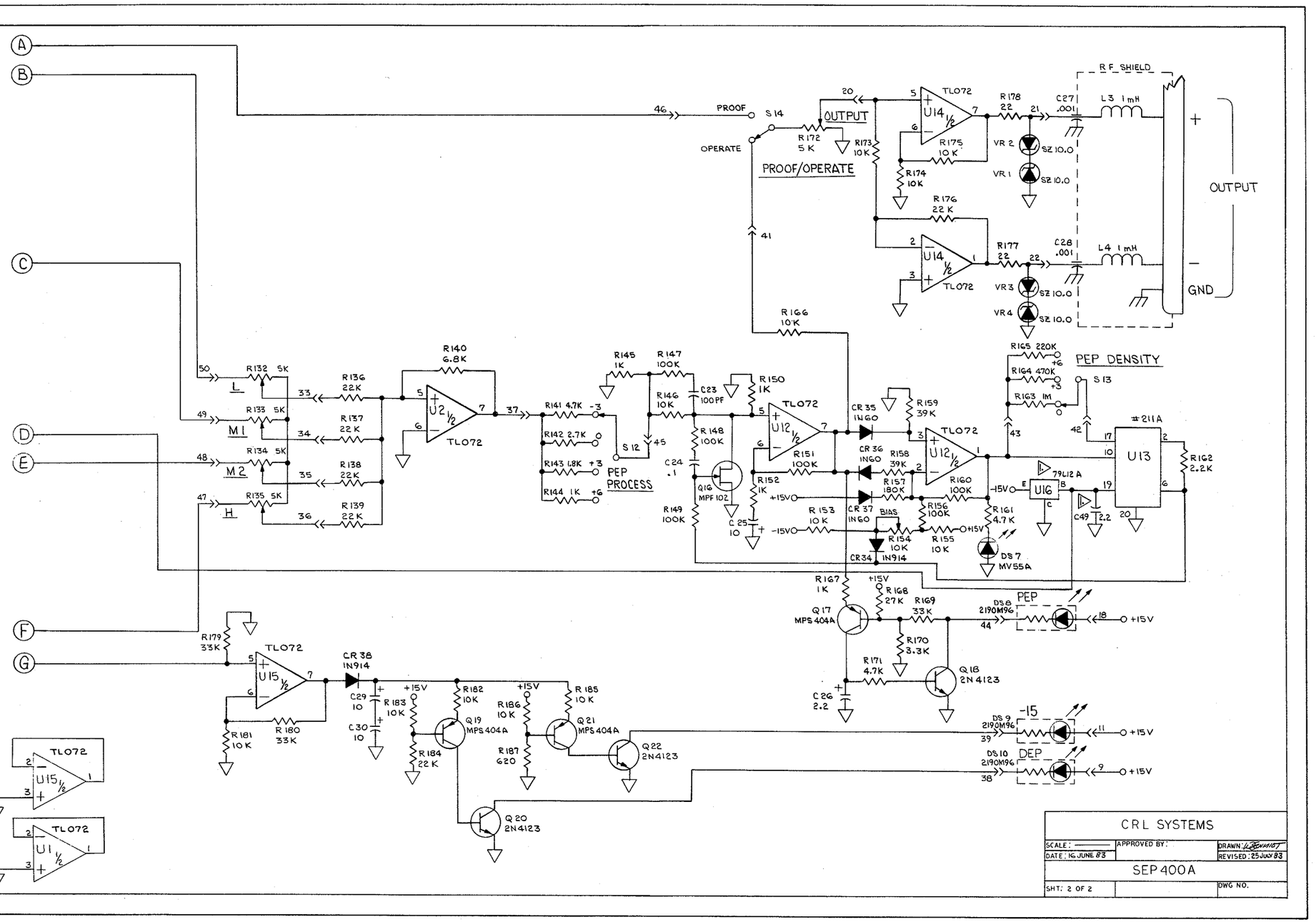


FIGURE 4.1 SEP-400A BLOCK DIAGRAM


INPUT
RF SHIELD
L1 1mH
L2 1mH
C1 .001
C2 .001
C3 10
C4 10
C5 10
C6 10
R198 4.7K
R197 4.7K
R1 620
R2 39K
R3 10K
R4 1K
R5 330K
R6 39K
R7 10K
R8 1K
R9 330K
R10 270
R11 5K
S1
S2
S3
S4
U1 1/2 TL072
INPUT
DEP PROCESS
R12 4.7K
R13 2.7K
R14 1.8K
R15 1K
R16 390
R17 1K
R18 22K
R19 33K
S5
U2 1/2 TL072
GATE
R20 1K
R21 10K
R22 3.3K
R23 100K
U3 1/2 TL072
R24 2.2K
R25 4.7K
R26 1M
R27 10K
R28 4.7K
CAL
DS1 2190M96
R30 330K
R196 180K
Q1 MPS 404A
Q2 2N4123
R31 8.2K
R32 4.7K
C8 2.2
GATE
DS2 2190M96
R33 22K
Q3 2N4123
R29 1K
WHITE
GREEN
BLACK
RF SHIELD
T1 SSA636
F1 3/10A
120 VAC 50/60 Hz
C31 .001
C32 .001
CR40
CR39
IN4001 (4)
CR42
CR41
C39 .01
C40 .01
C41 .01
C42 .01
C43 .01
C44 .01
C45 .01
C46 .01
C47 .01
C48 .01
R189 270
Q23 MPS U01
Q24 MJE 720
R190 1K
R188 390
VR5 SZ170A
C34 1000
R191 10K
CR43 IN4001
DS11 MV55A
C35 .22
R199 390
POWER
CR44 IN4001
Q26 MJE 710
R195 10K
DS12 MV55A
C36 .22
R194 1K
R193 270
Q25 MPS U51
R192 1K
VR6 SZ170A
C37 1000
C33 470
C36 470
DS 13 2190M94
L BAND
R34 8.2K
R35 100K
C9 .22
C10 .1
R36 100K
Q4 MPF 102
R37 100K
R38 22K
U4 1/2 TL072
R40 1K
C11 10
CR3 IN60
CR4 IN60
R39 100K
R47 39K
R46 39K
DS 3 MV55A
R51 4.7K
U4 1/2 TL072
R48 100K
+15 V
-15 V
R45 180K
BIAS
CR5 IN60
R44 100K
R41 10K
R42 10K
R43 10K
CR2 IN914
OFF
ON
S7
R50 1.8K
CR8 IN914
CR6 IN914
-15V
211A
U5
R49 1K
R53 1M
Q5 MPS 404A
Q6 MPS 404A
R54 2.2M
R55 1M
R57 22K
R56 22K
R52 10K
CR7 IN60
CR9 IN914
C12 .22
M1 BAND
R59 27K
R60 100K
R58 6.8K
C13 .01
R61 100K
C14 .1
Q7 MPF 102
R62 100K
R63 22K
U6 1/2 TL072
R65 1K
C15 10
CR11 IN60
CR12 IN60
R64 100K
R72 39K
R71 39K
DS 4 MV55A
R76 4.7K
U6 1/2 TL072
R73 100K
+15V
-15V
R70 180K
BIAS
CR13 IN60
R69 100K
R66 10K
R67 10K
R68 10K
CR10 IN914
OFF
ON
S8
R75 1.8K
CR16 IN914
CR14 IN914
-15V
211A
U7
R74 1K
R78 4.7M
Q8 MPS 404A
Q9 MPS 404A
R79 2.2M
R80 470K
R82 22K
R81 22K
R77 10K
CR15 IN60
CR17 IN914
M2 BAND
C16 .047
R84 22K
R83 4.7K
R85 100K
C17 .0022
R86 100K
Q10 MPF 102
R87 100K
R88 22K
U8 1/2 TL072
R90 1K
C19 10
C18 .1
CR19 IN60
CR20 IN60
R89 100K
R97 39K
R96 39K
DS 5 MV 55A
R101 4.7K
U8 1/2 TL072
R98 100K
+15V
-15V
R95 180K
BIAS
CR21 IN60
R94 100K
R91 10K
R92 10K
R93 10K
CR18 IN914
OFF
ON
S9
R100 1.8K
CR24 IN914
CR22 IN914
-15V
211A
U9
R99 1K
R103 4.7M
Q11 MPS 404A
Q12 MPS 404A
R104 2.2M
R105 470K
R107 22K
R106 22K
R102 10K
CR23 IN60
CR25 IN914
H BAND
C20 .0012
R109 100K
R108 33K
C21 .1
R110 100K
Q13 MPF 102
R111 100K
R112 22K
U10 1/2 TL072
R114 1K
C22 10
CR27 IN60
CR28 IN60
R113 100K
R121 39K
R120 39K
DS 6 MV55A
R125 4.7K
U10 1/2 TL072
R122 100K
+15V
-15V
R115 10K
R116 10K
R117 10K
CR26 IN914
OFF
ON
S10
R124 1.8K
CR32 IN914
CR30 IN914
-15V
211A
U11
R123 1K
R127 4.7M
Q14 MPS 404A
Q15 MPS 404A
R128 2.2M
R129 470K
R131 22K
R130 22K
R126 10K
CR31 IN60
CR33 IN914
+6
+3
-15V
17
S11
30
31
DEP DENSITY
A
B
C
D
E
F
G
COMPONENTS MOUNTED ON BOTTOM OF PRINTED CIRCUIT BOARD. R102, U16 AND C49.
CRL SYSTEMS
SCALE: ———
APPROVED BY:
DRAWN: L. SCHMIDT
DATE: 16 JUNE 83
REVISED: 25 JULY 83
SEP400A
SHT 1 OF 2
DWG NO.



CRL SYSTEMS		
SCALE: ———	APPROVED BY:	DRAWN: L. BROWNLOW
DATE: 16 JUNE 83		REVISED: 25 JULY 83
SEP 400A		
SHT: 2 OF 2		DWG NO.

CAPACITORS
ALL VALUES ARE IN MICROFARADS UNLESS OTHERWISE NOTED

C 1	.001 FEEDTHRU (+IN)	C 2	.001 FEEDTHRU (-IN)
C 3	10 ELECTROLYTIC 16V	C 4	10 ELECTROLYTIC 16V
C 5	10 ELECTROLYTIC 16V	C 6	10 ELECTROLYTIC 16V
C 7	10 ELECTROLYTIC 16V	C 8	2.2 TANTALUM 20% 16V
C 9	.22 POLYESTER 5% 100V	C 10	.1 POLYESTER 10% 100V
C 11	10 ELECTROLYTIC 16V	C 12	.22 POLYESTER 5% 100V
C 13	.01 POLYSTYRENE 5% 160V	C 14	.1 POLYESTER 10% 100V
C 15	10 ELECTROLYTIC 16V	C 16	.047 POLYESTER 5% 100V
C 17	.0022 POLYSTYRENE 5% 160V	C 18	.1 POLYESTER 10% 100V
C 19	10 ELECTROLYTIC 16V	C 20	.0012 POLYSTYRENE 5% 160V
C 21	.1 POLYESTER 10% 100V	C 22	10 ELECTROLYTIC 16V
C 23	100 PF CERAMIC 50V	C 24	.1 POLYESTER 10% 100V
C 25	10 ELECTROLYTIC 16V	C 26	2.2 TANTALUM 20% 16V
C 27	.001 FEEDTHRU (+OUT)	C 28	.001 FEEDTHRU (-OUT)
C 29	10 ELECTROLYTIC 16V	C 30	10 ELECTROLYTIC 16V
C 31	.001 FEEDTHRU	C 32	.001 FEEDTHRU
C 33	470 ELECTROLYTIC 50V	C 34	1000 ELECTROLYTIC 16V
C 35	.22 POLYESTER 10% 100V	C 36	470 ELECTROLYTIC 50V
C 37	1000 ELECTROLYTIC 16V	C 38	.22 POLYESTER 10% 100V
C 39	.01 POLYESTER 10% 100V	C 40	.01 POLYESTER 10% 100V
C 41	.01 POLYESTER 10% 100V	C 42	.01 POLYESTER 10% 100V
C 43	.01 POLYESTER 10% 100V	C 44	.01 POLYESTER 10% 100V
C 45	.01 POLYESTER 10% 100V	C 46	.01 POLYESTER 10% 100V
C 47	.01 POLYESTER 10% 100V	C 48	.01 POLYESTER 10% 100V
C 49	2.2 TANTALUM 20% 16V		

DIODES

CR 1	1N60	CR 2	1N914
CR 3	1N60	CR 4	1N60
CR 5	1N60	CR 6	1N914
CR 7	1N60	CR 8	1N914
CR 9	1N914	CR 10	1N914
CR 11	1N60	CR 12	1N60
CR 13	1N60	CR 14	1N914
CR 15	1N60	CR 16	1N914
CR 17	1N914	CR 18	1N914
CR 19	1N60	CR 20	1N60
CR 21	1N60	CR 22	1N914
CR 23	1N60	CR 24	1N914
CR 25	1N914	CR 26	1N914
CR 27	1N60	CR 28	1N60
CR 29	1N60	CR 30	1N914
CR 31	1N60	CR 32	1N914
CR 33	1N914	CR 34	1N914
CR 35	1N60	CR 36	1N60
CR 37	1N60	CR 38	1N914
CR 39	1N4001	CR 40	1N4001
CR 41	1N4001	CR 42	1N4001
CR 43	1N4001	CR 44	1N4001

LEDS

DS 1	2190M96 (CAL)	DS 2	2190M94 (GATE)
DS 3	MV55A (L BAND STATUS)	DS 4	MV55A (M1 BAND STATUS)
DS 5	MV55A (M2 BAND STATUS)	DS 6	MV55A (H BAND STATUS)
DS 7	MV55A (PEP STATUS)	DS 8	2190M96 (PEP)
DS 9	2190M95 (-15)	DS 10	2190M96 (DEP)
DS 11	MV55A (+15 STATUS)	DS 12	MV55A (-15 STATUS)
DS 13	2190M94 (POWER)		

FUSES

F 1	3/10 AMP SLO-BLOW		

COILS

L 1	1 MH	L 2	1 MH
L 3	1 MH	L 4	1 MH

TRANSISTORS

Q 1	MPS404A	Q 2	2N4123
Q 3	2N4123	Q 4	MPF102
Q 5	MPS404A	Q 6	MPS404A
Q 7	MPF102	Q 8	MPS404A
Q 9	MPS404A	Q 10	MPF102
Q 11	MPS404A	Q 12	MPS404A
Q 13	MPF102	Q 14	MPS404A
Q 15	MPS404A	Q 16	MPF102
Q 17	MPS404A	Q 18	2N4123
Q 19	MPS404A	Q 20	2N4123
Q 21	MPS404A	Q 22	2N4123
Q 23	MPSU01	Q 24	MJE720
Q 25	NDSU51	Q 26	MJE710

RESISTORS

ALL RESISTORS ARE 5% 1/4 WATT UNLESS OTHERWISE NOTED

R 1	620	R 2	39K
R 3	10K	R 4	1K
R 5	330K	R 6	39K
R 7	10K	R 8	1K
R 9	330K	R 10	270
R 11	5K MULTITURN POT	R 12	4.7K
R 13	2.7K	R 14	1.8K
R 15	1K	R 16	390

R 17	1K	R 18	22K
R 19	33K	R 20	1K
R 21	10K	R 22	3.3K
R 23	100K	R 24	2.2K
R 25	4.7K	R 26	1M
R 27	10K	R 28	4.7K
R 29	1K	R 30	330K
R 31	8.2K	R 32	4.7K
R 33	22K	R 34	8.2K
R 35	100K	R 36	100K
R 37	100K	R 38	22K
R 39	100K	R 40	1K
R 41	10K	R 42	10K TRIMPOT
R 43	10K	R 44	100K
R 45	180K	R 46	39K
R 47	39K	R 48	100K
R 49	1K	R 50	1.8K
R 51	4.7K	R 52	10K
R 53	1M	R 54	2.2M
R 55	1M	R 56	22K
R 57	22K	R 58	6.8K
R 59	27K	R 60	100K
R 61	100K	R 62	100K
R 63	22K	R 64	100K
R 65	1K	R 66	10K
R 67	10K TRIMPOT	R 68	10K
R 69	100K	R 70	180K
R 71	39K	R 72	39K
R 73	100K	R 74	1K
R 75	1.8K	R 76	4.7K
R 77	10K	R 78	4.7M
R 79	2.2M	R 80	470K
R 81	22K	R 82	22K
R 83	4.7K	R 84	22K
R 85	100K	R 86	100K
R 87	100K	R 88	22K
R 89	100K	R 90	1K
R 91	10K	R 92	10K TRIMPOT
R 93	10K	R 94	100K
R 95	180K	R 96	39K
R 97	39K	R 98	100K
R 99	1K	R 100	1.8K
R 101	4.7K	R 102	10K
R 103	4.7M	R 104	2.2M
R 105	470K	R 106	22K
R 107	22K	R 108	33K
R 109	100K	R 110	100K
R 111	100K	R 112	22K
R 113	100K	R 114	1K
R 115	10K	R 116	10K TRIMPOT
R 117	10K	R 118	100K
R 119	180K	R 120	39K
R 121	39K	R 122	100K
R 123	1K	R 124	1.8K
R 125	4.7K	R 126	10K
R 127	4.7M	R 128	2.2M

R 129 470K
R 130 22K
R 131 22K
R 132 5K POT (L)
R 133 5K POT (M1)
R 134 5K POT (M2)
R 135 5K POT (H)
R 136 22K
R 137 22K
R 138 22K
R 139 22K
R 140 6.8K
R 141 4.7K
R 142 2.7K
R 143 1.8K
R 144 1K
R 145 1K
R 146 10K
R 147 100K
R 148 100K
R 149 100K
R 150 1K
R 151 100K
R 152 1K
R 153 10K
R 154 10K TRIMPOT
R 155 10K
R 156 100K
R 157 180K
R 158 39K
R 159 39K
R 160 100K
R 161 4.7K
R 162 2.2K
R 163 1M
R 164 470K
R 165 220K
R 166 10K
R 167 1K
R 168 27K
R 169 33K
R 170 3.3K
R 171 4.7K
R 172 5K MULTITURN POT
R 173 10K
R 174 10K
R 175 10K
R 176 22K
R 177 22
R 178 22
R 179 33K
R 180 33K
R 181 10K
R 182 10K
R 183 10K
R 184 22K
R 185 10K
R 186 10K
R 187 620
R 188 390
R 189 270
R 190 1K
R 191 10K
R 192 1K
R 193 270
R 194 1K
R 195 10K
R 196 180K
R 197 4.7K
R 198 4.7K
R 199 390

SWITCHES

S 1 1/4 MINI DIPSWITCH
S 2 1/4 MINI DIPSWITCH
S 3 1/4 MINI DIPSWITCH
S 4 1/4 MINI DIPSWITCH
S 5 ROTARY (DEP PROCESS)
S 6 105E TOGGLE (GATE)
S 7 1/4 MINI DIPSWITCH
S 8 1/4 MINI DIPSWITCH
S 9 1/4 MINI DIPSWITCH
S 10 1/4 MINI DIPSWITCH
S 11 ROTARY (DEP DENSITY)
S 12 ROTARY (PEP PROCESS)
S 13 ROTARY (PEP DENSITY)
S 14 105D TOGGLE (PRF/OPER)

TRANSFORMERS

T 1	SSA636

ICS

U 1	TL072	U 2	TL072
U 3	TL072	U 4	TL072
U 5	211A	U 6	TL072
U 7	211A	U 8	TL072
U 9	211A	U 10	TL072
U 11	211A	U 12	TL072
U 13	211A	U 14	TL072
U 15	TL072	U 16	79L12A

ZENERS

VR 1	SZ10.0	VR 2	SZ10.0
VR 3	SZ10.0	VR 4	SZ10.0
VR 5	SZ17.0	VR 6	SZ17.0